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DESIGN OF A RECONFIGURABLE PIPELINED ARCHITECTURE FOR SRC FILTER FOR SOFTWARE RADIO RECEIVER

ASHOK AGARWAL & LAKSHMI BOPANNA

Department of Electronics and Communication Engineering, National Institute of Technology, Warangal, Telangana, India

ABSTRACT

In the receiver architecture of Software Defined Radio (SDR) channelization and sample rate conversion (SRC) are the two computational intensive tasks. CIC filters can be employed to achieve sample rate changes by integral factors but needs a gain compensation filter and fractional rate SRC to achieve the required sample rate. In this paper a pipelined architecture for the SRC employing joint compensation and interpolation, discrete compensation and interpolation method is simulated in Xilinx ISE 14.7 and implemented on KINTEX-7 XC7K325t-2FFG900 FPGA. The design is tested for four standards, viz., GSM900, CDMA2000, WCDMA and HiperLAN using Virtual Input Output Cores and Integrated Logic analyzers on Kintex-7 board. Comparison of two methods show that discrete compensation and interpolation outperforms when compared with joint compensation and interpolation technique at the cost of increased latency.

KEYWORDS: CIC Filter, DDC, Farrow Structure, Fpgas, IF, Interpolation, Symbol Rate, RF, SRC